// Verilog test fixture created from schematic D:\Xilinxproject\xxl\xxl1.sch - Sun Oct 08 23:39:42 2017

`timescale 1ns / 1ps

module xxl1\_xxl1\_sch\_tb();

// Inputs

reg A0;

reg A1;

reg A2;

// Output

wire B0;

wire B1;

// Bidirs

// Instantiate the UUT

xxl1 UUT (

.A0(A0),

.A1(A1),

.A2(A2),

.B0(B0),

.B1(B1)

);

// Initialize Inputs

`ifdef auto\_init

initial begin

A0 = 0;

A1 = 0;

A2 = 0;

`endif

initial

begin

A0=0;A1=0;A2=0;

#400;$stop;

end

always #50 A0=~A0;

always #100 A1=~A1;

always #200 A2=~A2;

endmodule